A CMOS CURRENT-MODE SQUARER/RECTIFIER CIRCUIT

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ABSTRACT

In this paper, a new current squarer and precision full-wave rectifier based on a CMOS class AB amplifier that modified to receive a differential input current has been presented. The proposed circuits are simulated with HSPICE level 49. From a ±1.5V supply voltage, the power consumption of the rectifier and the squarer at the quiescent point are about 210nW and 120μW, respectively. The total harmonics distortion of the squarer is less than 1%, with a input signal of 24μA.

1. INTRODUCTION

Squarer and full-wave rectifier are useful importance basic building block for the design of many analog signal processing applications, communications, frequency translation and instrumentation systems.

Usually, a squarer circuit can be realized by through the use of the square-law characteristics of MOS transistor [1][2][3]. For a full-wave rectifier circuit, it can be realized by some arrangement of diode-operational amplifier, diode-current conveyor, CMOS class AB amplifier and translinear current conveyor [8][6][4][5]. The main disadvantages of the mentioned methods are that they require a large power supply voltage, high power dissipation and large circuit implementations. Another problem is the accuracy. For the rectification, an interesting circuit, which is based on the class AB amplifier has been proposed [4], where it needs a large magnitude of the input current supplied by the input voltage and a resistor that cause an error for very low input current.

In this paper, a low voltage, current-mode and compact circuit structure precision squarer/full-wave rectifier have been introduced.

2. CIRCUIT DESCRIPTION

2.1 Class AB Amplifier

Consider a CMOS class AB amplifier formed by transistors M_1, M_2, M_3 and M_4 shown in Fig.1, where the current source I_{DD} provides the bias current for the circuit. Assuming that all transistors M_1, M_2, M_3 and M_4 are matched and are biased in saturation region with individual wells connected to their sources to eliminate the body effect [3]. Connecting the input node Y to a constant voltage and applying the input current I_x, we can express the drain currents of the transistors M_3 and M_4 as [4][7]

$$I_{d3} = \frac{(4I_{DD} - I_x)^2}{16I_{DD}} \quad \text{for } |I_x| \le 4I_{DD} \qquad (1)$$

$$I_{d4} = \frac{(4I_{DD} + I_x)^2}{16I_{DD}} \quad \text{for } |I_x| \le 4I_{DD} \qquad (2)$$

The expressions (1)-(2) are valid when the four transistors stay in saturation mode. However, if we apply the magnitude of the input current $|I_x| \ge 4I_{DD}$, the drain current I_{D3} close to zero and the transistor M_3 will be cut off. Then, the input current flows through the transistor M_4. This means that this circuit functions as a half-wave rectifier.

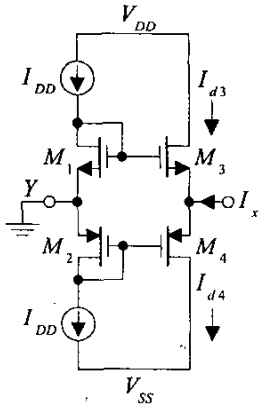

Fig. 1 CMOS class AB amplifier.

2.2 Current-Mode Squarer/Rectifier Circuit

Fig. 2 shows the current squarer/rectifier circuit. The proposed circuit consists of the CMOS class AB amplifier which is modified to receive the differential input current $\pm I_{in}$. The current gain of the p-type current mirror M_7-M_8 is unity. Assuming that the complementary pair of transistors M_1-M_2, M_3-M_4 and M_5-M_6 are identical. Neglecting the body effect and if all of the transistors are biased in

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saturation region, by applying eqns.(1)-(2), we can express the drain currents I_{d3} and I_{d5} as

$$I_{d3} = I_{DD} - \frac{I_{in}}{2} + \frac{I_{in}^2}{16 I_{DD}} \quad (3)$$

$$I_{d5} = I_{DD} + \frac{I_{in}}{2} + \frac{I_{in}^2}{16 I_{DD}} \quad (4)$$

The summation of the drain currents I_{d3} and I_{d5} is copied by the p-type current mirror M_7 and M_8, then the output current I_o can be written as

$$I_o = (I_{d3} + I_{d5}) - 2I_{DD} \quad (5)$$

$$= \frac{I_{in}^2}{8 I_{DD}} \quad \text{for } |I_{in}| \le 4 I_{DD} \quad (6)$$

It is clearly seen that the output current I_o is related to the square of the input current I_{in}, where the squarer factor can be controlled by the bias current I_{DD}, as indicated by eqn.(6).

On the other hand, if we select the bias current $I_{DD} \le I_{in}/4$, then the circuit will operate in class B mode. This means that [4]

$$I_o = I_{D5} = I_{in} \quad \text{for } I_{in} > 0 \quad (7)$$

$$I_o = I_{D3} = I_{in} \quad \text{for } I_{in} < 0 \quad (8)$$

Therefore, the output current I_o becomes

$$I_o = |I_{in}| \quad (9)$$

In this case, the circuit represents a current full-wave rectifier.

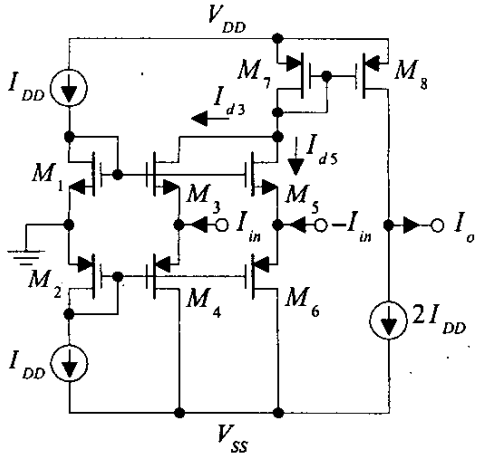

Fig. 2 Current squarer/rectifier circuit.

The complete current-mode squarer and full-wave rectifier circuit is shown in Fig.3. Where, the current sources I_{DD} and $2I_{DD}$ were replaced by the transistors M_8, M_{12} and M_{11}, respectively. The transistors M_{13}-M_{15} and M_7 generate the bias current for the class AB cell M_1-M_6.

From the proposed circuit of Fig.3, the squarer and rectifier functions can be achieved by connecting or by opening the drain-to-source of the transistor M_{15}. If the drain-to-source of M_{15} is not connected together and $(V_{DD}\text{-}V_{SS}) \le (V_{TN13} + |V_{TP14}| + |V_{TP15}| + |V_{TP17}|)$, where V_{TN} and V_{TP} are the threshold voltage of NMOS and PMOS transistors, respectively. The circuit works as a full-wave rectifier.

Finally, by connecting the drain-to-source of the transistor M_{15} together, the value of $(V_{DD}\text{-}V_{SS}) \le (V_{TN13} + |V_{TP14}| + |V_{TP7}|)$, and all the transistors are biased in saturation region, the proposed circuit becomes a squarer.

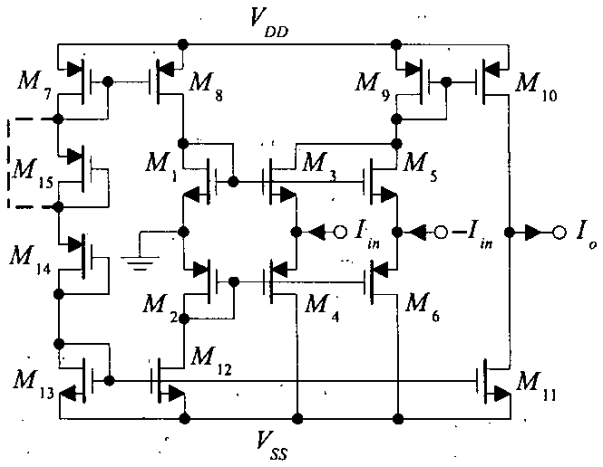

Fig. 3 Complete current squarer/rectifier circuit.

MOS transistor	$W(um)$	$L(um)$
M_1, M_3, M_5	10	5
M_2, M_4, M_6	32	5
$M_7 - M_{10}$	60	5
M_{11}	73	5
M_{12}, M_{13}	40	5
M_{14}, M_{15}	30	5

Table 1. Transistor sizes used in the squarer/rectifier circuit.

3. SIMULATION RESULTS

The proposed squarer/rectifier circuit of Fig.3 was simulated by HSPICE using the model parameter of HP 0.5μm CMOS process level 49. The transistor dimensions

are given in Table 1. To cancel out the dc output offset current, the aspect ratio of the transistor M_{11} must be adjusted. The bulks(body) of all transistors are connected to respective power supply V_{DD} and V_{SS}, that is ±1.5V.

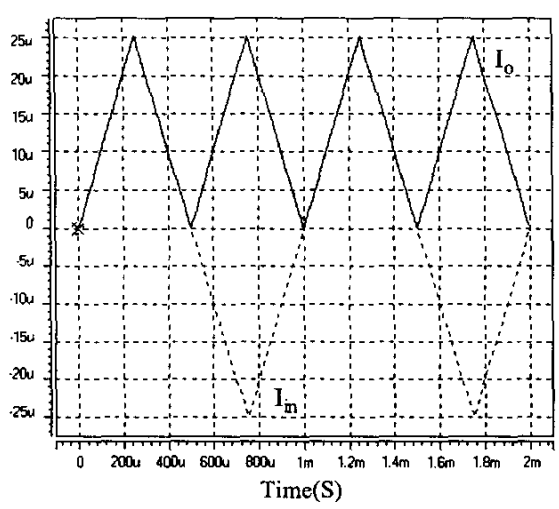

Fig. 4 Triangular differential input current.

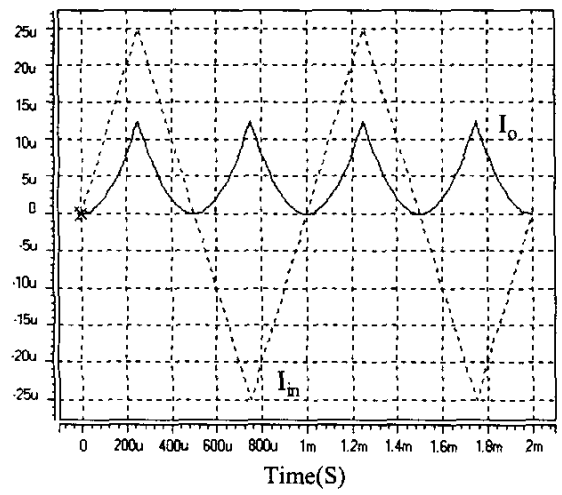

Fig. 5 Simulated current squarer response.

Fig.4 shows the response for the use of rectification function, by applying the triangular differential input current with peak amplitude of 25μA and the frequency is 1kHz, the drain of M_{15} is not connected to source. The bias currents of the transistors M_1-M_6 that the value of 12nA have been measured and the power dissipation at the bias point is about 210nW.

By connecting the drain-to-source of M_{15}, the bias currents of M_1-M_6 is set to 6.6μA and, the power consumption is about 120μW, respectively. Now the circuit works as a squarer and the output current waveform can be observed in Fig.5.

The total harmonics distortion (THD) against a 1kHz input current is shown in Fig.6 and has been calculated as the harmonic content of the fundamental frequency at 2kHz [1]. THD value less than 1% is achieved for the input current <24μA. The THD versus the output frequency with a 24μA input current signal is shown in Fig.7. It is lower than 1.1% up to 1MHz.

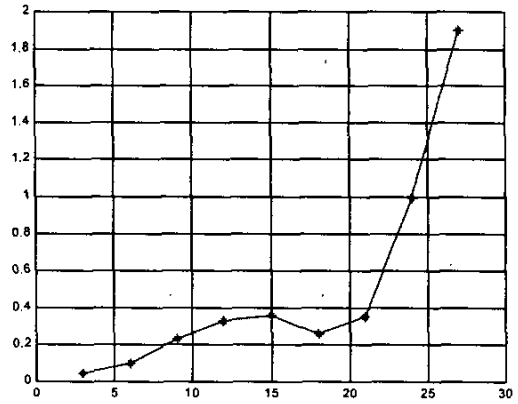

Fig. 6 THD against input current.

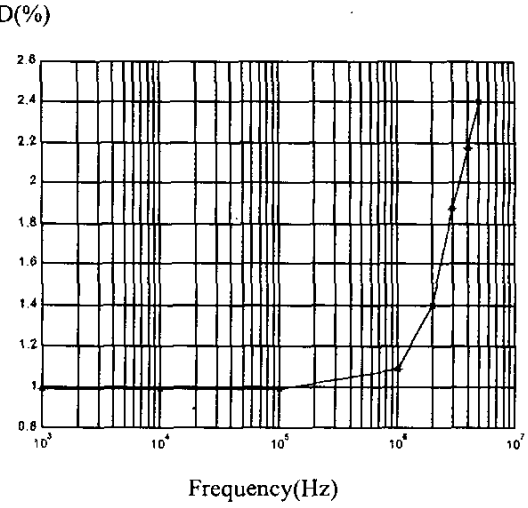

Fig. 7 THD against output frequency.

4. CONCLUSION

The realization of current-mode squarer and full-wave rectifier in the same circuit based on the use of a modified CMOS class AB amplifier has been proposed. Their performances have been demonstrated by the HSPICE program.

ACKNOWLEDGEMENT

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